24.6 A 14:1 Dynamic MUX FF with Select Activity Detection

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High-performance multimedia processors generally use forwarding techniques to increase pipeline processing efficiency. In general, a processor that simultaneously executes multiple instructions has many forwarding paths. In the specific processor discussed in this paper, the number of paths is 14 [1]. A dynamic MUX FF reduces both the area and delay of the combined 14:1 MUX and FF in the execution stage of the processor [2, 3], which places the following two requirements on the 14:1 MUX FF:

(1) The MUX FF needs to hold the stored data of pipeline registers in the next cycle in its non-enabled state, which occurs if none of the enable signals are active. This happens when the pipeline is stalled by a cache miss, a data hazard, a control hazard, etc.

(2) The MUX FF must steadily output the expected value, even if some of the enable signals of the MUX (i.e., multi-enable states) are selected to raise fault coverage in scan test mode.

In cases of a pipeline stall, conventional dynamic MUX FFs cannot hold the previous value because of the non-enabled state. Moreover, in multimedia processors for a mobile world, the low-power operation of a MUX FF is essential. In this paper, a dynamic MUX FF with fast detection of enable states that addresses the above issues, is described.

Figure 24.6.1 shows the proposed MUX FF circuit that consists of four components: the actual path (Actual), the replica path (Replica), the output path (Output & Hold), and the scan path (Scan). In the Actual path in which the structure adopts cascaded dynamic circuits, 14b data (D[13:0]) and enable signals (E[13:0]) are applied into the first dynamic circuit (1stAD). AD1 of 1stAD is connected to the gates of both an NMOS (M1) of the second dynamic circuit (2ndAD) and the static NOR logic (S-NOR) to transmit only the setup data during the evaluation phase (CK=H). The Replica path, the key point of the proposed MUX FF, features the following two items. First, Replica holds the previous data of Output & Hold in the non-enabled state; i.e., after the dynamic circuit of the first replica (1stRD1) keeps RD1 “H” by fast detecting E[13:0]=L, the RD2 of the second dynamic circuit of the replica (2ndRD) remains “L” until the precharge phase. Second, the 1stRD1 guarantees the timing of the evaluate switch (M2) on 2ndAD; that is, the rising edge of RD1# is slower than the falling edge of AD1 despite the enable states, because 1stRD involves only one active NMOS (i.e., the gate connected to the input SEB) and has extra wire capacitance between the top and the middle NMOS devices. Scan has an advantage of easily handling the hold time of the scan input data (SI) at the scan shift mode (SEB=L), because the circuit has almost the same structure as the other static FF used in the processor.

Figure 24.6.2 shows the simulated waveform of the proposed MUX FF. The first cycle is a normal single-enable pattern (E[0]=H, E[13:1]=L), the second cycle is a no-enable pattern (E[13:0]=L), and the third cycle is a multi-enable pattern (E[13:0]=H). A single-enable pattern shows that the proposed MUX FF structure helps avoid transitions on Q, even if D[0] changes from “L” to “H” while both CK and E[0] are “H”. The no-enable pattern confirms that MUX FF holds the previous value “L” by RD2. The multi-enable pattern shows that MUX FF operates steadily because of the safety delay time between the rising edge of RD1# and the falling edge of AD1. In addition, since MUX FF is sequentially precharged in the order of RD1 and AD1 and both AD2 and RD2, the glitch of output Q does not happen regardless of PVT variation.

Figure 24.6.3 shows the cell layout structure of 1stAD and 1stRD. The upper NMOS devices for 1stRD have the same structure as the lower NMOS devices for 1stAD and are surrounded at the top and on both sides by NWELL. The structure helps guarantee the time difference between the rising edge of RD1# and the falling edge of AD1, because NMOS V_t shifts as a function of distance for well edges [4]. The structure also reduces the parasitic capacitance of E[13:0]. Moreover, the devices for the tie circuit that protect the gate from ESD, are inserted into the left side of the NWELL. The tie circuit arrangement within the cell has stronger noise immunity from crosstalk noise than the external arrangement.

Figure 24.6.4 depicts a block diagram showing an evaluation of the MUX FF setup time and CK-Q delay. The slew of each input can be changed continuously by a 4b register. Both input and output signals of MUX FF are connected to the proposed slew detectors, that consist of three domino circuits in which the V_t of input NMOS (M3) is fine tuned by the Vbn of high-resolution body bias [5]. Both the power supply voltage V_{DD}[3:1] and V_{SS}[3:1] for the three domino circuits are shifted up every 100mV. When the rising edge of the Q of MUX FF reaches $V_{DD}/2$, the domino circuit output (DOUT[2]) begins to fall. The time difference of each falling edge of DOUT[3:1] during the evaluation phase (ϕ0=L) is measured using the phase difference of the rising edge of the three clocks (ϕ1, 2, 3) on each FF. Therefore, the slew value can be defined by a straight-line approximation of the time difference. In addition, the slew detector has a function for sensing a reversed transition, which is caused by crosstalk noise, that detects the rising edge of DOUT# during the evaluation phase (DOUT=L).

Figure 24.6.5 shows the measurement results of CK-Q delay versus setup time. The measurement condition is V_{DD}=1.2V at 25°C, the process is typical, and input signal slew=100ps. The measured plot is the average data of 50 chips. In cases above setup time of –100ps, CK-Q delay is very close to the simulated data. In cases below setup time of –100ps, CK-Q delay differs from the simulated data, because they depend on a simulator algorithm.

Figure 24.6.6 compares the proposed MUX FF versus other conventional FFs, including static CMOS and XCFF types [2] that added a 14:1 static MUX with a holding function to the input data of each FF. The comparison includes power consumption at different activity ratios as well as the area and delay from input D[13:0] and E[13:0] to output Q. The area is reduced by 70% compared to that of conventional FFs, and the delay is improved by 50%. The power consumption of the MUX FF is reduced to 12% of that of conventional FFs where each signal activity ratio=10. Thus, the proposed MUX FF is especially effective for data paths with forwarding paths for a multimedia processor. Fig. 24.6.7 shows a chip micrograph for evaluating these FFs. The chip is fabricated in a 90 nm LP CMOS triple-well process.

References:

[1] M. Nakajima, et al., “Instruction Parallel Processor (IPP) Architecture on Panasonic Integrated Platform for Digital CE,” *Spring Processor Forum*, May, 2005.

[2] A. Hirata, et al., “The Cross Charged-control Flip-Flop: a Low-Power and High-Speed Flip-Flop Suitable for Mobile Application SoCs,” *Symp.VLSI Circuits*, pp. 306-307, Jun., 2005.

[3] F. Klass, et al., “A New Family of Semidynamic and Dynamic Flip-Flops with Embedded Logic for High-Performance Processors,” *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 712 -715, May, 1999.

[4] T. Hook, et al., “Proximity Effects and VLSI Design,” *ICICDT*, pp. 166-169, May 2005.

[5] M. Sumita, “High Resolution Body Bias Techniques for Reducing the Impacts of Leakage Current and Parasitic Bipolar,” *ISLPED*, pp. 203-208, Aug., 2005.

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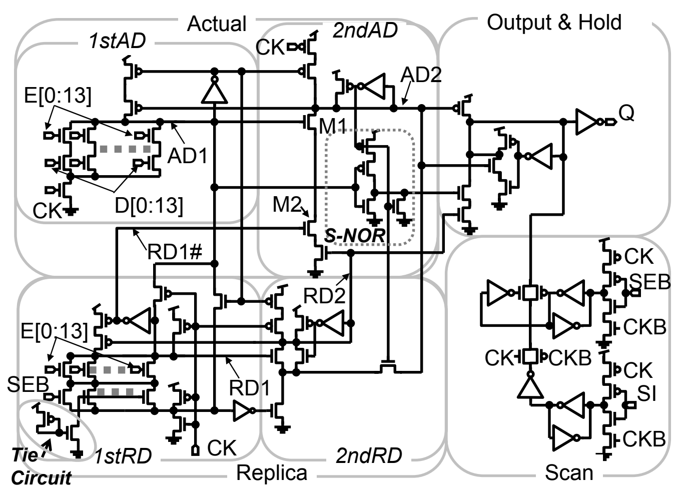


Figure 24.6.1: Proposed MUX FF circuit.

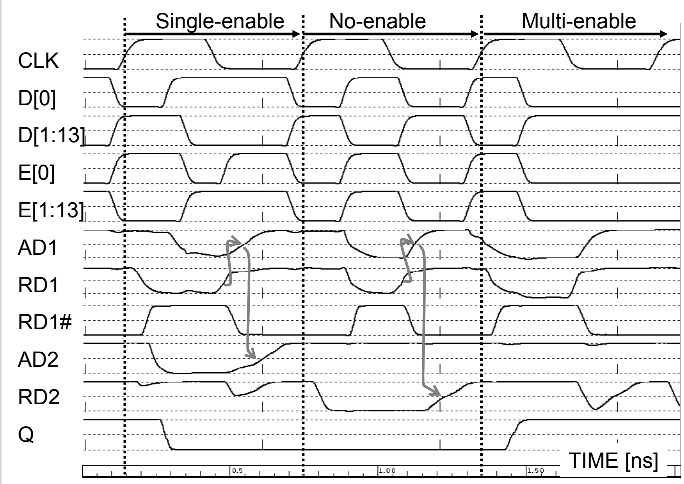


Figure 24.6.2: Simulated waveform of proposed MUX FF.

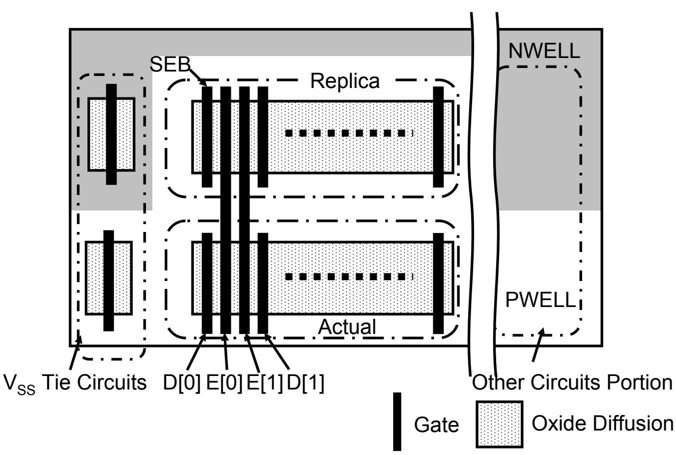


Figure 24.6.3: Proposed MUX FF layout structure.

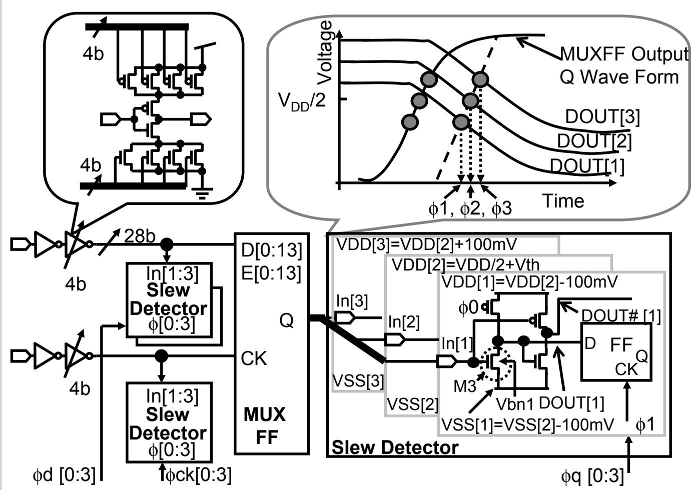


Figure 24.6.4: Block diagram for evaluating MUX FF and other FFs.

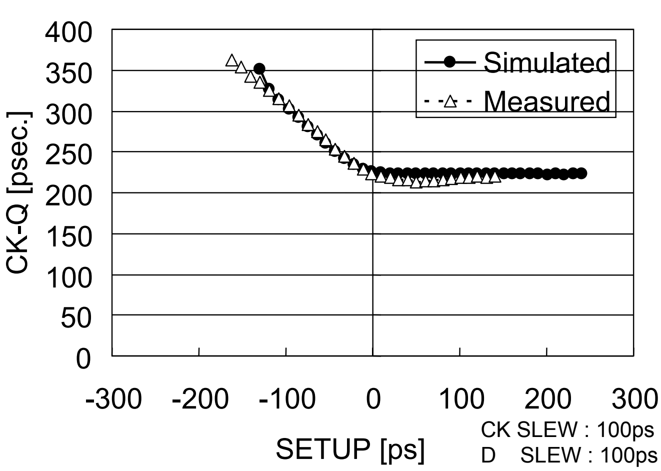
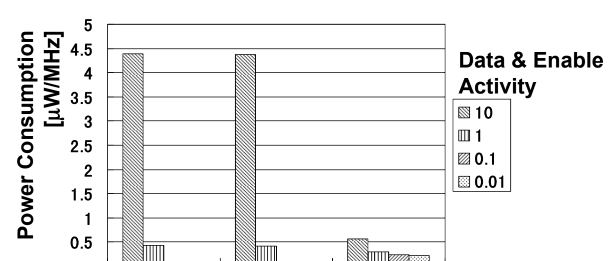


Figure 24.6.5: Measured CK-Q delay versus setup time.



	D-FF	XCFF[2]	MUX FF
Area [μm²]	182	184	130
E-Q [ps]	427	372	182
D-Q [ps]	374	300	146

CK SLEW : 100ps
D SLEW : 100ps

V_{DD}=1.2V, T=25ºC, Process Typ.
A Inverter delay=44ps @ F.O.=4
Measured.

Figure 24.6.6: Comparison of proposed MUX FF versus other FFs with MUX.

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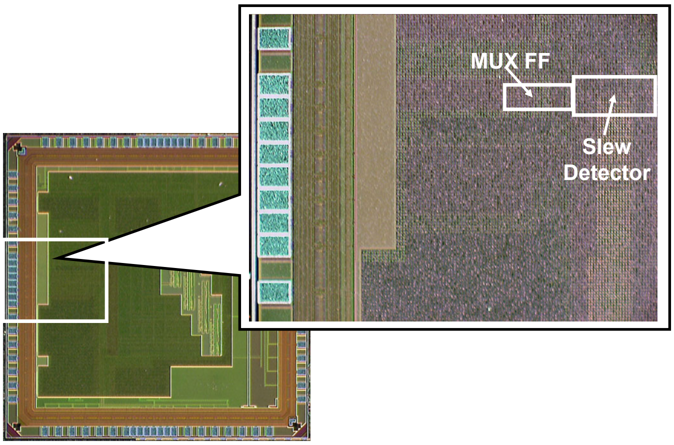

Figure 24.6.7: Chip micrograph.

